How to build a netlist from a schematic (built with SARC Editor).

The SARC algorithm is capable to process a description of a linear circuit or a SW circuit.

An example of a linear circuit :

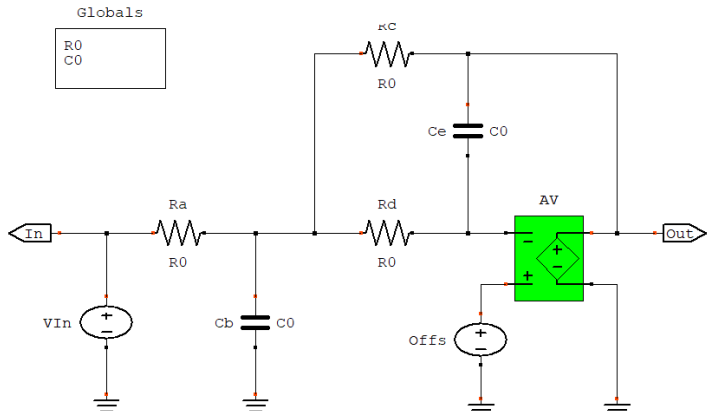

figure 1

An example of a SW circuit :

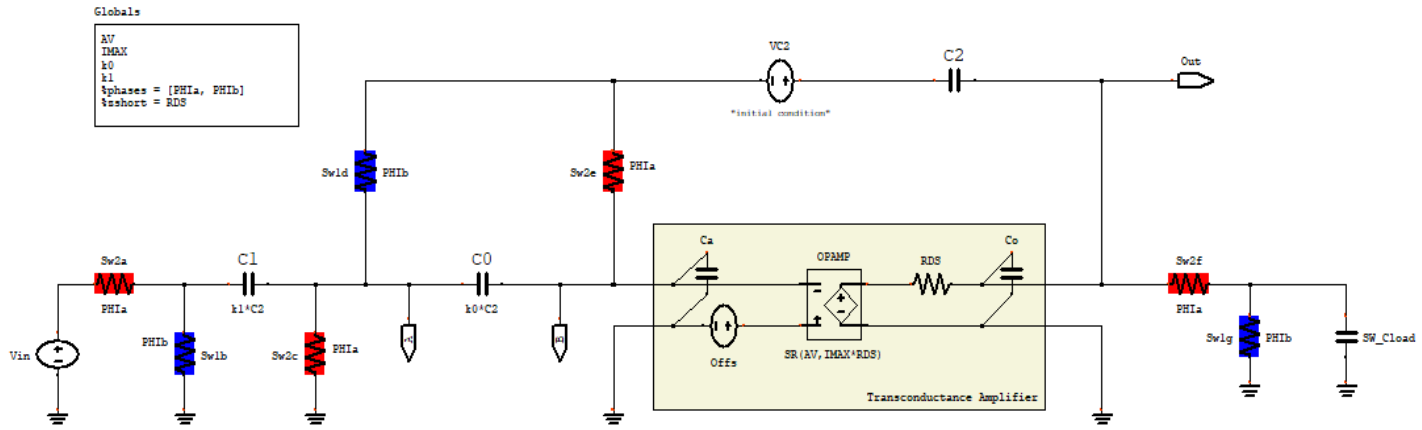

figure 2

Both descriptions use the same basic 9 linear elements :

V *(voltage source)*
I *(current source)*
R *(resistance)*
L *(inductance)*
C *(capacitance)*
E *(voltage controlled voltage source)*
G *(voltage controlled current source)*
H *(current controlled voltage source)*
F *(current controlled current source)*

The circuits are built within the **SARC Schematic Editor :**

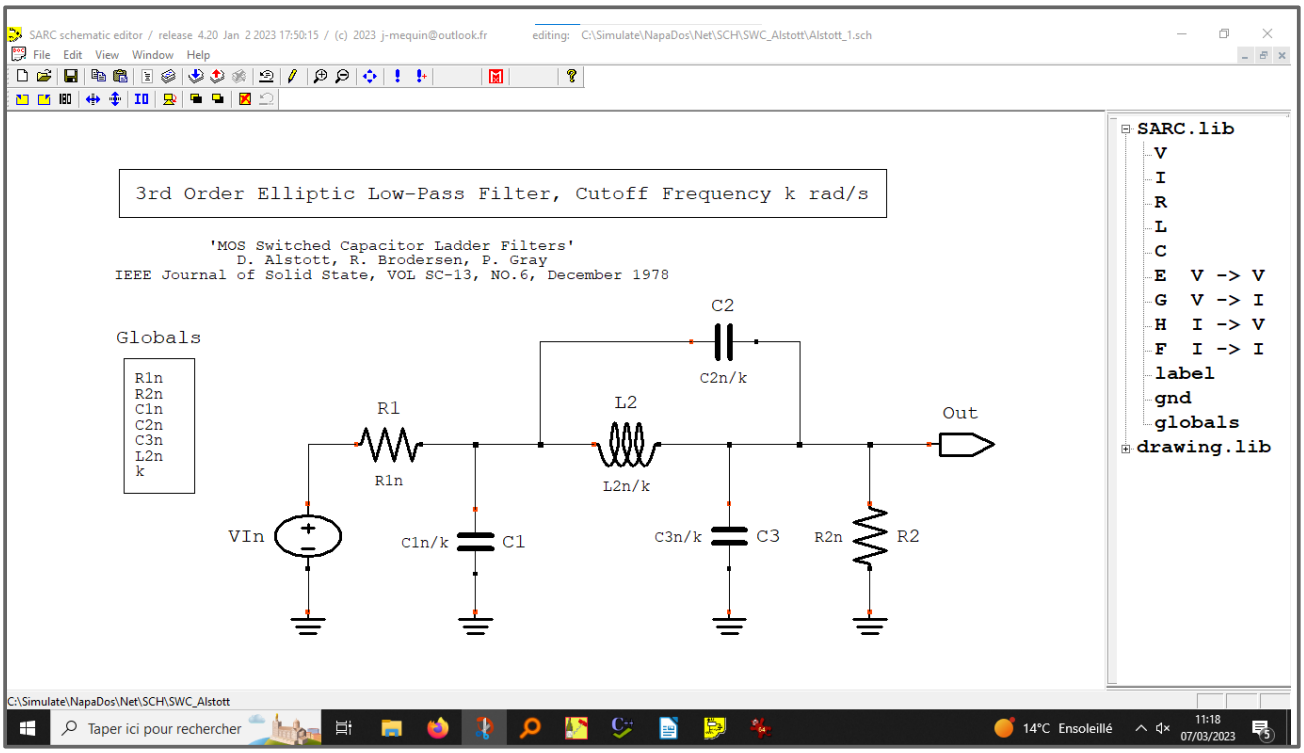

Figure 4

But the description of SW circuit has a few particularities.

First, the controlled source E is the only controlled source allowed in the description if a Z model has to be produced.

As we intend to use the same schematic to produce a Z model and a quasi-linear model for SW circuits, some elements must be qualified according to the model to be produced.

The switches are represented as resistors. But their resistance will vary from a very small to a very large value following the 2 phases ot the driving clock during the simulation.

%phases declares specifically these 2 phases. The cycle is automatically defined as the succession of the 2 phases in the order of their declaration.

Resistive elements interacting with capacitances induce time constants. These resistors must be hidden in the Z model. This is the role of the **%zshort** or **%zopen** declarations.

Globals

```
AV
IMAX
k0
k1
%phases = [PHIa, PHIb]
%zshort = RDS
```

Figure 3

In the SARC Schematic Editor, the setup can be configured to create automatically the Napa cells modeling the circuit for the time continuous linear circuits or SW circuits.

A few WxMaxima functions are made availbale to the user to simplify the building of the NAPA cells :

SARC simulation for time-continuous circuits, 2 or 4 phases SW circuits

MIMO_CELL( ) ;

ZTRANS simulations for simulations using the Z model of 2 phases SW circuits

Z1_CELL(‘an output signal’) ; Z model (cycle level)
Z2_CELL(‘an output signal’) ; Z model (phase level)